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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,031	11/19/2003	Mark L. DiOrio	MTB005US1P	7148

27906 7590 11/21/2006

PATENT LAW OFFICES OF DAVID MILLERS
6560 ASHFIELD COURT
SAN JOSE, CA 95120

EXAMINER	
PATEL, PARESH H	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 11/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/718,031	DIORIO, MARK L.	
	Examiner	Art Unit	
	Paresh Patel	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,13 and 15-33* is/are pending in the application.

4a) Of the above claim(s) *4-6 and 16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-10,13,15,17-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06/05, 07/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Species of fig. 9E, claims 1-3, 5, 7-10, 10, 15, 17-33 in the reply filed on 09/11/2006 is acknowledged. Applicant believes that claims 5, 8, 9 and 23 read on elected species and claims 4, 6 and 16 read on non-elected species. Since claim 5 depends from claim 4, claim 5 is withdrawn from consideration.

Response to Arguments

2. Applicant's arguments, see pages 6-7 of Remarks, filed 05/24/2006, with respect to the rejection(s) of claim(s) 1-10, 10 and 15-33 under 35 USC §102 and §103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Ahn et al. and Komari.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 7-10, 13, 15, 17-18, 22-23 and 27-33 rejected under 35 U.S.C. 102(b) as being anticipated by Komori (US 6480012).

Regarding claims 1 and 29-33, Komori discloses all the elements including a probing system for testing a device comprising:

a probe [1, 23] comprising a semiconductor die [13] and probe tips [plurality of 21] rigidly attached to the semiconductor die, wherein probe tips comprises bumps (suitable for flip chip) [plurality of 21] arranged in a pattern that matches a pattern of terminals [plurality of 26 of 33] on the device [33 of 4] and that directly contact the terminals during testing of the device; and

a tester [tester, not shown] electrically connected to the probe tips [via 6].

Regarding claim 2, Komori discloses the device comprises a semiconductor material [silicon] that is substantially the same as material in the semiconductor die [silicon].

Regarding claim 3, Komori discloses a probe card [2] including a receptacle [for 1] in which the probe is detachably mounted, wherein the tester makes electrical connections to the probe tips through the probe card.

Regarding claim 7, Komori discloses the semiconductor die comprises: terminals [17, see fig. 15] on a bottom surface of the semiconductor die; and

conductive vias [44 in 35, also see element 36 in 28 of fig. 11 in Ahn et al. US 6379982] that pass through the semiconductor die and provide electrical connections between the probe tips on a top surface of the die and the terminals on the bottom surface.

Regarding claim 8, Komori discloses the probe further comprises a substrate [23] on which the semiconductor die is mounted, wherein the terminals of the semiconductor die directly contact the substrate.

Regarding claim 9, Komori discloses a probe card [2], wherein terminals on the substrate directly contact the probe card.

Regarding claim 10, Komori discloses positioning system [see fig. fig. 13] adapted to position the probe relative to the device so that the probe tips contact the terminals on the device.

Regarding claim 13, Komori inherently discloses (see rejection of claim 7 above, because forming steps are inherent there) a method for forming a probe for electrical testing of a semiconductor device, comprising:

forming probe tips on a semiconductor die in a pattern matching a pattern of terminals on the semiconductor device; and

fabricating an interconnect structure for electrical connection of the probe tips to test equipment, as further claimed.

Regarding claim 15, Komori discloses, wherein fabricating the interconnect structure comprises forming conductive traces on a surface of the semiconductor die on which the probe tips reside [this steps are inherent to rejection of claim 7 above].

Regarding claim 17, Komori discloses, wherein fabricating the interconnect structure comprises forming conductive vias through the semiconductor die, the vias respectively being in electrical contact with the probe tips [this steps are inherent to rejection of claim 7 above].

Regarding claim 18, Komori discloses forming holes and filling the holes with a conductive material [this steps are inherent to the rejection of claim 7 above].

Regarding claim 22, Komori discloses forming terminals, as further claimed [this steps are inherent to the rejection of claim 7 above].

Regarding claim 23, Komori discloses attaching the terminals to an interconnect [this steps are inherent to the rejection of claim 7 above].

Regarding claims 27-28, Komori discloses similar manufacturing process for die and the device as claimed.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 19-21 and 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Komori as applied to claims 18, 17 and 13 above.

Regarding claims 19-20, Komari discloses all the elements but is silent about forming the holes comprises laser drilling or etching. Rather, Komari discloses a holes [see fig. 15 for 35]. Forming the holes in the wafer are well known in the art (see fig. 11 of Ahn et al. US 6379982). It would have been obvious matter of a design choice to use well known laser or chemical etching to make a holes for interconnect purpose, since applicant has not disclosed that use of laser or etching solves any stated problems or is

for any particular purpose and it appears that the invention would perform equally well with the holes as created by Komori.

Regarding claim 21, Komori discloses all the elements but is silent about forming the conductive vias comprises forming doped regions that extend through the semiconductor die. However, forming the conductive vias comprises forming doped regions that extend through the semiconductor die is well known in the art (see fig. 11 of Ahn et al. US 6379982). Therefore, It would have been obvious matter of a design choice to use well known process to make conductive path, since applicant has not disclosed that forming of doped regions solves any stated problems or is for any particular purpose and it appears that the invention would perform equally well with the via 25 of Komori.

Regarding claim 24, Komori discloses all the elements but is silent about a solder reflow process. Use of solder reflow process is well known in the interconnect art (see fig. 11 of Ahn et al. US 6379982). Therefore, It would have been obvious matter of a design choice to use well-known process to make conductive path, since applicant has not disclosed that this process solves any stated problems or is for any particular purpose and it appears that the invention would perform equally well with the terminal of Komori.

Regarding claims 25-26, Komori discloses all the elements but is silent about planarizing the bumps and polishing of the bumps. Since these processes are well known in the art for its intended purpose, it would have been obvious to one having

ordinary skill in the art at the time the invention was made to planarzing and polishing the bumps as further claimed for simultaneous contact with the device during testing.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paresh Patel whose telephone number is 571-272-1968. The examiner can normally be reached on 8:00 to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Paresh Patel 11/17/06
Primary Examiner
Art Unit 2829

November 17, 2006